IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of
SUGIHARA ET AL.
Serial No. 10/560,907
Filed: December 16, 2005

Confirmation No. 2364
Atty. Ref.: LB-1035-616
TC/A.U.: 2815
Examiner: Kim, Jay C.

For: SEMICONDUCTOR DEVICE, MANUFACTURING METHOD THEREOF, AND ELECTRONIC DEVICE

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Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

RULE 132 DECLARATION OF TOSHINORI SUGIHARA

Pursuant to Rule 132, I hereby declare as follows:

1. I, Toshinori Sugihara, am employed by Sharp Kabushiki Kaisha, headquartered in Osaka, Japan, one of the assignees of the above-listed patent application. I am also listed as an inventor on the instant patent application.

2. My current job at Sharp involves Liquid Crystal Display.

3. I respectfully submit that the range for the threshold voltage of the gate voltage, cited in claim 4 of the 10/560,907 application, achieves unexpected results over the prior art ranges, thus the cited prior art's teachings would not have made it obvious to one of ordinary skill in the art at the time the invention was made to intentionally add nitrogen and hydrogen dopants having concentrations so that a threshold voltage of a gate voltage

of the semiconductor device is controlled to be substantially in a range between 0V and 3V.

A TFT having a protective layer has its threshold voltage shifted to an unpractical range, see p. 15, line 12 to p. 18, line 16 and Fig. 15 of the instant specification. The invention of claim 4 addresses this problem by employing an arrangement in which nitrogen and hydrogen are so doped that a threshold voltage of the TFT is in a practically usable range of 0V to 3V, even though the device employs a protective layer.

In a TFT having a protective layer, an interface level of a ZnO layer in back channel can be reduced. In contrast, in a TFT having no protective layer, an interface level of a ZnO layer in back channel (defect level of a ZnO layer on back channel surface) causes much more band-bending on a back channel side, resulting in the number of carriers (free electrons) being reduced. In the TFT having no protective layer, the band-bending on the back channel side extends up to the channel side, and this therefore causes a polarity of the channel to be i-type. Thus, a threshold voltage of the TFT having no protective layer is in a practical range (2V to 5V).

On the other hand, in a TFT having a protective layer, the interface level of a ZnO layer in back channel is reduced, and therefore no or very little band-bending is caused in the ZnO layer. Therefore, the ZnO layer can exist in an original state, i.e., a state in which free electrons generated from oxygen deficiencies are large in number. As such, a polarity of the channel is n-type. The increased number of the free electrons has to be removed in order for the TFT to be turned off. As shown in Fig. 16 of the instant specification, such an increase of the carriers which causes the threshold voltage of the

TFT to be a large negative voltage is explained by the phenomenon in which the resistivity is shifted and largely reduced by providing a protective layer in the TFT.

In the TFT of the invention of claim 4 (having a protective layer), nitrogen and hydrogen are so doped that the number of the free electrons as carriers is reduced. Further, the doping of nitrogen and hydrogen causes the Fermi level to move and get close to the center of the band gap. This allows a decrease of the gate voltage required for removal of the too many free electrons. This makes it possible to obtain a threshold voltage of the TFT that is in a practical range of 0V to 3V, which is far away from the expected range of large negative values (around -30V), which occurs for TFT's with a protective layer.

4. I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

Respectfully submitted,

Date: April 7, 2011 By: Toshinori Sugihara
Toshinori Sugihara